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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,929	03/31/2001	John T. Orchard	012.P10008	7551

43831 7590 08/10/2007

BERKELEY LAW & TECHNOLOGY GROUP, LLP
17933 NW Evergreen Parkway, Suite 250
BEAVERTON, OR 97006

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
08/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	09/823,929	ORCHARD, JOHN T.
	Examiner	Art Unit
	Chat C. Do	2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-9,11-19 and 22-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,7-9,11-19 and 22-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/30/2007.

2. Claims 2-5, 7-9, 11-19, and 22-49 are pending in this application. Claims 2, 17, 32, and 44 are independent claims. In Amendment, claims 1, 6, 10, and 20-21 are previously cancelled. This Office Action is made non-final after a RCE filed 05/30/2007.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 2-5, 7-9, 11-19, and 22-49 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 2-5, 7-9, 11-19, and 22-49 cite a method and apparatus for performing sum of partial products in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 2-5, 7-9, 11-19, and 22-49 merely disclose steps/components for performing sum of partial products without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad

and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 2-5, 7-9, 11-19, and 22-49 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 44-46 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Grisamore (U.S. 6,535,901).

Re claim 44, Grisamore discloses in Figures 1, 4-5, and 7 an apparatus (e.g. Figure 1 and abstract) comprising: a summing module generator (e.g. part 14, 16, and 18 in Figure 1), summing module generator being adapted to: receive input terms (e.g. 1st current multiplicand 20 and 2nd current multiplicand 22 in Figure 1); perform bit-wise analysis of the input terms (e.g. col. 2 lines 35-40 and col. 3 lines 42-47); and dynamically configure a summing module (e.g. through reduction tree module 14 in Figure 1), wherein the summing module, as configured, comprises: a hybrid Wallace tree comprising one or more elements (e.g. col. 2 lines 62-68), wherein the elements comprise one or more adders having one or more associated registers and one or more additional registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each

adder for pipelining and col. 1 lines 36-38), wherein the Wallace tree comprises a reduced number of elements to perform summing operations on the one or more input terms (e.g. col. 1 lines 42-47 and col. 2 lines 62-68); and a integrated multi-input adder (e.g. adder 18 in Figure 1 as general and components 14, 16, and 18 as specific) configured to combine summation results produced by the hybrid Wallace tree (e.g. Figure 1 and col. 1 lines 42-58).

Re claim 45, Grisamore further discloses in Figures 1, 4-5, and 7 the one or more adders comprise one or more full-adders and one or more half-adders (e.g. col. 3 lines 42-47).

Re claim 46, it is an apparatus claim of claim 3. Thus, claim 46 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 49, Grisamore further discloses in Figures 1, 4-5, and 7 the hybrid Wallace tree is dynamically configured, wherein the configurations based at least in part on one or more properties of the input terms (e.g. col. 3 lines 42-49).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-5, 7-9, 11-12, 17-19, 22-27, and 47-48 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claim 2, Grisamore discloses in Figures 1, 4-5, and 7 an apparatus comprising: a plurality of first inputs to receive multiple input terms (e.g. 1st current multiplicand 20 and 2nd current multiplicand 22 in Figure 1); a device coupled with the plurality of inputs (e.g. component 12 in Figure 1); and a summing module generator (e.g. 14 and 16 in Figure 1) coupled with the dedicated logic device, wherein the summing module generator is adapted to structure the dedicated logic device to implement a multi-stage summing module comprising one or more full-adders and associated registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 36-40 and col. 3 lines 55-61; and inherently), half-adders (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 36-40 and col. 3 lines 55-61; and inherently), and single registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 1 lines 36-38; and inherently), wherein the summing module is adapted to produce intermediate summation results (e.g. output of reduction tree module 14 as 1st preceding resultant 26 and 2nd preceding resultant 28) by combining the multiple input terms (e.g. partial product terms from generator 12) according to a pipelined reduction pattern (e.g. col. 1 lines 32-41, col. 2 lines 35-42, and col. 3 lines 20-27), wherein the summing module generator is further adapted to implement an integrated multi-input adder into the summing module, wherein the integrated multi-input adder (e.g. 18 as adder in Figure 1)

includes a plurality of second inputs (e.g. as feedback as seen in Figure 1 with components 26 an d28), wherein at least a portion of the plurality of second inputs are adapted to receive feedback input of accumulator bits (e.g. feedback from memory 16 in Figure 1) from one or more of the full-adders and associated registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 36-40 and col. 3 lines 55-61; and inherently), half-adders and associated registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 36-40 and col. 3 lines 55-61; and inherently), and single registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 1 lines 36-38; Figure 5 illustrates the single registers as registers that store/latch the value directly from above) of the summing module and wherein the integrated multi-input adder is further adapted to produce a final sum (e.g. multiplied accumulated resultant 34) of the input terms by combining the intermediate summation results (e.g. output of 14). Grisamore does not disclose a dedicated logic device couple to the summing module. However, Chang et al. disclose the series of Boolean function generators as a summing module is coupled with a dedicated logic device comprising a FPGA (e.g. 2nd paragraph on the left column page 309). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the summing module couple with a dedicated logic device as seen in Chang et al.'s invention into Grisamore's invention because it would enable to reduce the hardware cost for performing logic functions (e.g. 2nd paragraph on the left column page 309).

Re claim 3, Grisamore further discloses in Figures 1, 4-5, and 7 the multiple input terms include one or more accumulator bits (e.g. 26 and 28 wherein each of these bits is the resultant bit of previous or preceding summation).

Re claim 4, Grisamore does not the dedicated logic device comprises a plurality of Boolean function generators, wherein the Boolean function generators comprise four-input look-up tables (LUTs) to implement Boolean logic functions. However, Chang et al. disclose in Figure 1(a) Boolean function generator comprise four-input look-up tables (LUTs) to implement Boolean logic functions (e.g. left column page 310 lines 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a LUTs to implement Boolean logic functions as seen in Chang's invention into Grisamore's invention because it would enable to reduce the hardware cost (e.g. introduction section on page 309 lines 7-15).

Re claim 5, Grisamore further discloses in Figures 1, 4-5, and 7 the Boolean function generator pairs with an associated register to form the atomic structure of a dedicated logic device (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 1 lines 36-38).

Re claim 7, Grisamore further discloses in Figures 1, 4-5, and 7 the multi-input adder comprises an adder (e.g. adder 18 in Figure 1) with an input for each single register in a final stage of the multiple stages of the summing module (e.g. col.3 lines 60-63 and Figure 5 layer 2).

Re claim 8, Grisamore further discloses in Figures 1, 4-5, and 7 the integrated multi-input adder includes a plurality of single registers to receive feedback accumulator

bits (e.g. 26 and 28 in Figure 1 and Figure 5 layer 6 as feedback from layer 2) from the multi-input adder, the accumulator bits resulting from a multiply-accumulate operation (e.g. output of 18 in Figure 1).

Re claim 9, Grisamore further discloses in Figures 1, 4-5, and 7 an accumulator coupled with the multi-input adder to feed the accumulator bits back into the summing module (e.g. feedback from output of 16 to input of reduction tree module 14 in Figure 1).

Re claims 11-12, Grisamore does not disclose in Figures 1, 4-5, and 7 the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA and a device with control logic and a block of dedicated logic. However, Chang et al. disclose the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA (e.g. 2nd paragraph on the left column page 309) and a device with control logic and a block of dedicated logic (e.g. control signals for controlling the block of hardware). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to implement the Boolean function generators in a dedicated logic device comprising a FPGA with control logic and a block of dedicated logic as seen in Chang et al.'s invention into Grisamore's invention because it would enable to reduce the hardware cost for performing logic functions (e.g. 2nd paragraph on the left column page 309).

Re claim 17, it is a method claim of claim 2. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 18, it is a method claim of claim 3. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 19, it is a method claim of claim 4. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 22, it is a method claim of claim 7. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 23, it is a method claim of claim 8. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 24, it is a method claim of claim 9. Thus, claim 24 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 25, it is a method claim of claim 2. Thus, claim 25 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 26, it is a method claim of claim 11. Thus, claim 26 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 27, it is a method claim of claim 12. Thus, claim 27 is also rejected under the same rationale in the rejection of rejected claim 12.

Re claims 47-48, they have same limitations as cited in claims 11-12. Thus, claims 47-48 are also rejected under the same rationale in the rejection of rejected claim 11-12.

9. Claims 13-16 and 28-31 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for

discrete function transforms using LUT-based FPGAs"), as applied to claims 2 and 17 above, in view further of Fang et al. ("A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations").

Re claims 13-16, Grisamore in view of Chang disclose in Figures 1, 4-5, and 7 an FPGA architecture to implement the one or more full-adders (e.g. Figure 3), half-adders (e.g. Figure 2), and single registers (e.g. col. 1 lines 35-40 and col. 3 lines 42-48), the architecture based at least in part on an analysis of the input terms (e.g. col. 2 lines 35-40) comprising a bit-wise analysis (e.g. col. 2 lines 33-35). Grisamore in view of Chang do not disclose in Figures 1, 4-5, and 7 a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically (e.g. left column 3rd paragraph page 1189 and Module1(DP) in Figure 3 and Figure 1) structures the atomic elements of the dedicated logic device (e.g. Figure 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device as seen in Fang's invention into Grisamore in view of Chang's invention because it would enable an operator to dynamically program or configure a specific function in low manufacturing time and cost (e.g. first paragraph in the introduction section).

Re claim 28, it is a method claim of claim 13. Thus, claim 28 is also rejected under the same rationale in the rejection of rejected claim 13.

Re claim 29, it is a method claim of claim 14. Thus, claim 29 is also rejected under the same rationale in the rejection of rejected claim 14.

Re claim 30, it is a method claim of claim 16. Thus, claim 30 is also rejected under the same rationale in the rejection of rejected claim 16.

Re claim 31, it is a method claim of claim 15. Thus, claim 31 is also rejected under the same rationale in the rejection of rejected claim 15.

10. Claims 32, 36-38, and 42-43 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979).

Re claim 32, Grisamore discloses in Figures 1, 4-5, and 7 a method for performing arithmetic comprising: generating a plurality of partial products from two or more input terms (e.g. partial product generator 12 in Figure 1); that implements in one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the partial products (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 35-40); determining the structure of the Boolean function generators based, at least in part, on one or more attributes of the input terms (e.g. col. 8 lines 20-30); receiving in both branches accumulator bits over a feedback path (e.g. 26 and 28), wherein the accumulator bits are respectively provided to an integrated multi-input adder; and adding (e.g. adder 18 in Figure 1) the intermediate summation results with the accumulator bits for each branch to produce a final components sum (e.g. output of adder 18 in Figure 1). Grisamore does not implicitly disclose two paths one for a real-

component branch, inverting certain partial products and passing the inverted and non-inverted partial products and one for an imaginary-component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously. However, Greenberger clearly discloses in Figure 2 a complex arithmetic operation comprising two paths (e.g. real and imaginary wherein label with Zr and Zi) one for a real-component branch (e.g. left side of Figure 2) inverting certain partial products (e.g. 34.1 for subtraction) and passing the inverted and non-inverted partial products and one for an imaginary-component branch (e.g. right side of Figure 2), passing the partial products (e.g. 34.2 for addition). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add two paths one for a real-component branch, inverting certain partial products and passing the inverted and non-inverted partial products and one for an imaginary-component branch, passing the partial products as seen in Greenberger's invention into Grisamore's invention because it would enable to reduce the complexity of processing the complex operands and the area in an integrated circuit (e.g. col. 3 lines 38-42 and col. 4 lines 45-52).

Re claim 36, Grisamore further discloses in Figures 1, 4-5, and 7 generating a plurality of partial product terms comprises combining the two or more inputs in a combinatorial stage of a complex multiply accumulator (e.g. Figure 1 as multiplication).

Re claim 37, Grisamore further discloses in Figures 1, 4-5, and 7 analyzing one or more attributes of the input terms (e.g. col. 2 lines 35-40).

Re claim 38, Grisamore further discloses in Figures 1, 4-5, and 7 analyzing the one or more attributes of the input terms comprises performing a bit-wise analysis of the

input terms (e.g. col. 2 lines 33-35 wherein the bit-wise is logical function of the partial products).

Re claim 42, Grisamore further discloses in Figures 1, 4-5, and 7 the multi-stage series of Boolean function generators are pipelined (e.g. Figure 5 wherein the reduction stage goes from high to low; e.g. 6, 4, 2… and col. 1 lines 32-41).

Re claim 43, Grisamore further discloses in Figures 1, 4-5, and 7 the partial products of the two or more input terms are reduced according to a pattern structured (e.g. col. 2 lines 35-43) by partitioning bits of equal significance into groups of three to be passed as inputs to the full-adders, remaining groups of two to be passed ms inputs to the half-adders (e.g. col. 8 lines 20-30), and remaining single bits to be passed to single registers (e.g. col. 5 lines 48-53).

11. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979), as applied to claim 32 above, in further view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claims 33-35, Grisamore in view of Greenberger do not disclose in Figures 1, 4-5, and 7 the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA and a device with control logic and a block of dedicated logic. However, Chang et al. disclose the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA (e.g. 2nd paragraph on the left column page 309) and a device with control logic and a block of dedicated logic (e.g. control

signals for controlling the block of hardware. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to implement the Boolean function generators in a dedicated logic device comprising a FPGA with control logic and a block of dedicated logic as seen in Chang et al.'s invention into Grisamore in view of Greenberger's invention because it would enable to reduce the hardware cost for performing logic functions (e.g. 2nd paragraph on the left column page 309).

12. Claims 39-41 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979) in further view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs"), as applied to claim 37 above, and in further view of Fang et al. ("A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations").

Re claims 39-41, Grisamore in view of Greenberger in further view of Chang et al. disclose in Figures 1, 4-5, and 7 a dedicated logic architecture to implement the one or more full-adders (e.g. Figure 3), half-adders (e.g. Figure 2), and single registers (e.g. col. 1 lines 35-40 and col. 3 lines 42-48), the architecture based at least in part on an analysis of the input terms (e.g. col. 2 lines 35-40) comprising a bit-wise analysis (e.g. col. 2 lines 33-35). Grisamore in view of Greenberger in further view of Chang et al. do not disclose in Figures 1, 4-5, and 7 a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically (e.g. left column 3rd paragraph page 1189 and Module1(DP) in Figure 3 and Figure 1) structures the atomic elements of the

dedicated logic device (e.g. Figure 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device as seen in Fang's invention into Grisamore in view of Greenberger in further view of Change et al.'s invention because it would enable an operator to dynamically program or configure a specific function in low manufacturing time and cost (e.g. first paragraph in the introduction section).

Response to Arguments

13. Applicant's arguments filed 05/30/2007 have been fully considered but they are not persuasive.

a. The applicant argues in page 10 for claims 44-46 and 49 rejected under 35 U.S.C. 102 that the cited reference by Grisamore fails to disclose a hybrid Wallace tree comprising one or more elements which comprises one or more adders having one or more associated registers and one or more additional registers.

The examiner respectfully submits that the argued limitations above is clearly seen in the cited reference, particularly Figure 5 of the cited reference. As previously mentioned and clearly addressed above rejection, the pipeline architecture design needs plurality of registers at optimal points in the array multiplier (e.g. as array adders within the multiplier to sum all the partial products of the multipler) as seen in Figure 5. In Figure 5 of the cited reference, it discloses at least one of half-adder (e.g. an adder for adding two inputs to yield a

sum in columns 3 and 6 first stage in dot-circuit) with its associated register (e.g. the register to store result of the half-adder sum where the arrow points to the second stage); at least one full-adder (e.g. an adder for adding more than two inputs to yield a sum in columns 4-5 in first stage for adding three inputs) and its associated register (e.g. the register to store the result of the full adder in the next stage); and at least an additional register (e.g. register which store the value directly from above stage, for example registers in column 1 of second stage for storing direct values of registers in column 1 of the first stage).

b. The applicant argues in page 11 for claims rejected under 35 U.S.C. 102 that the cited reference by Grisamore fails to disclose the integrated multi-input adder wherein the integrated multi-input adder is defined in the specification as an accumulator bits are introduced into registers in the summing module.

The examiner respectfully submits that the claims do not clearly specific the integrated multi-input adder as argued by the applicant referring back to the specification. Even taking the consideration of definition in the specification, the cited reference by Grisamore discloses the integrated multi-input adder as an integrated adder by components 14, 16, and 18 in Figure 1 wherein these components basically fulfill or meet all the limitations cited by the applicant's definition of the integrated multi-input adder.

c. The applicant argues in pages 12-13 last and first paragraph for claim 2 that the cited primary reference fails to disclose the summing module generator is adapted to structure the dedicated logic device to implement a multi-stage summing module.

The examiner respectfully submits that Figure 5 of the primary reference along with citation clearly shows the above argued limitations wherein Figure 5 discloses a physically and logically way to add multiple partial products in an unique way to yield final result as sum of partial product in Figure 5.

d. The applicant argues in page 13 last paragraph for claim 2 that the primary reference fails to disclose one or more adders having one or more associated registers and one or more additional registers.

The examiner respectfully submits that the argued limitations above is clearly seen in the cited reference, particularly Figure 5 of the cited reference. As previously mentioned and clearly addressed above rejection, the pipeline architecture design needs plurality of registers at optimal points in the array multiplier (e.g. as array adders within the multiplier to sum all the partial products of the multipler) as seen in Figure 5. In Figure 5 of the cited reference, it discloses at least one of half-adder (e.g. an adder for adding two inputs to yield a sum in columns 3 and 6 first stage in dot-circuit) with its associated register (e.g. the register to store result of the half-adder sum where the arrow points to the second stage); at least one full-adder (e.g. an adder for adding more than two inputs to yield a sum in columns 4-5 in first stage for adding three inputs) and its

associated register (e.g. the register to store the result of the full adder in the next stage); and at least an additional register (e.g. register which store the value directly from above stage, for example registers in column 1 of second stage for storing direct values of registers in column 1 of the first stage).

e. The applicant argues in page 12 for claim 2 that the primary reference fails to disclose a summing module adapted to produce intermediate summation result by combining the multiple input terms.

The examiner respectfully submits that the argued limitations are seen in Figures 1 and 5 of the primary reference. The summing module is including components 14, 16, and 18 in Figure 1 and structurally arrange as seen in Figure 5 for producing two vectors as feedback to one of the input of the integrated multi-input adder.

f. The applicant argues in page 15 first and second paragraphs for claim 2 that the primary reference fails to disclose an integrated multi-input adder including a plurality of inputs some of which receive feedback.

The examiner respectfully submits that Figure 1 discloses an integrated multi-input adder as components 14, 16, and 18 in Figure including a plurality of inputs from the partial product generator some of which receive feedback as feedback from components 16 wherein the intermediate summation result is the feedback signal from the integrated adder.

g. The applicant argues in page 16 first paragraph for claim 2 that the secondary reference discloses a FPGA to implemented summing module not an FPGA coupled to a summing module.

The examiner respectfully submits that the secondary reference by Change clearly discloses a FPGA couple to the summing module in second paragraph on the left column page 309.

h. The applicant argues in page 16 last paragraph for claim 3 that the primary reference fails to disclose the multiple input terms include one or more accumulator bits.

The examiner respectfully submits that the multiple input terms are terms input into the adder reduction tree 14 wherein the accumulator bits are the feedback signals 26 and 28.

i. The applicant repeatedly argues in pages 17-20 for claims that previously argue as seen above.

The examiner respectfully refers the applicant backs to the previous responses above corresponding to the argument.

j. The applicant argues in page 21 for claim 32 that the secondary reference fails to disclose the negating certain partial products and simultaneously passing the negated and non-negated partial products to a multi-stage series of Boolean function generators.

The examiner respectfully submits that the negated and non-negated partial products are inherently occurred depending on the input operands. If the input operand is negative, then the partial product will be negated partial product or vice versa which can be inherently disclosed in the primary reference, however, the secondary reference is used to further support the rejection which disclose a path of passing the generated partial products to the summing module.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

k. U.S. Patent No. 7,007,059 to Mohammed et al. disclose a fast pipelined adder/subtractor using increment/decrement function with reduced register ultilization.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Chat C. Do
Examiner
Art Unit 2193

August 6, 2007